ENCODER/DECODER ARCHITECTURE AND RELATED PROCESSING SYSTEM

ABSTRACT OF THE DISCLOSURE

An encoder/decoder architecture for buses, capable of minimizing power consumption by reducing the switching activity, generates, from an input information value relating to a given instant, a corresponding current output value on encoded bus lines relating to the same given instant. The architecture including storage device for storing respective preceding values of input information and output information relating to instants preceding the aforesaid given instant. A prediction block generates, from the preceding value of input information, an estimate of the current input information value. A decorrelation block decorrelates the current input information value with respect to the said estimate. A selection block selects as the current output value one out of the current input information value, the result of the decorrelation implemented by the decorrelation block or the preceding output value.